IN THE SPECIFICATION

Amendments to the Specification:

Please replace the paragraph [012] with the following rewritten paragraph:

--A commonly used IC layout used to fabricate the dual port core cell shown in Fig. 3 is illustrated in Fig. 4. Approximately 2/3^{rds} of the cell's area comprises an p-type ~~n-type~~ substrate 43 for the fabrication of n-type transistors and the other 1/3rd of the cell's surface area comprises a n-type ~~p-type~~ substrate 45 for the fabrication of p-type transistors. These n-type and p-type transistors are then coupled together to form inverters 21. Trace 41 in Fig. 4 indicates the areas of the cell that are interconnected to form one of the inverters. Metal interconnections are run through and across the cell to various points, creating the bit lines, the word lines and the power and ground lines. The metal interconnections are not illustrated in Fig. 4.--

Please replace the paragraph [030] with the following rewritten paragraph:

-- Fig. 5 illustrates the final device layout of a core cell fabricated according to the first embodiment of the present invention. Core cell 100 is fabricated upon a substrate of first p [[n]]-type substrate 101, first n [[p]]-type substrate 103 and second p [[n]]-type substrate 105. Two ~~pnp~~ pmos transistors 107 are fabricated on substrate 103 and 6 nmos ~~npn~~ transistors 109 are fabricated on substrates 101 and 105. The process steps required to fabricate these transistors are known and require no further description here. Black areas in Fig. 5 indicate where a via has been made from the various overlying metal layers (see Fig. 6), which form the ground, V_{DD} and bitlines, into the diffusion layer or polysilicon layer of the underlying transistors. The formation of these vias is conventional and does not require discussion here.--